GENERATION OF A GUARD INTERVAL IN A DMT MODULATION TRANSMISSION

CROSS-REFERENCE TO RELATED APPLICATION

This application is a continuation of U.S. Patent Application No. 09/491,685, filed January 26, 2000, now pending, which application is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to discrete multitone modulation (DMT), and more specifically, to the generation of cyclic prefixes in a DMT modulation transmission. The DMT modulation is for example used by standards ADSL and ADSL-lite.

Discussion of the Related Art

In a DMT modulation, data coded in the form of complex frequency coefficients are, on the transmit side, translated into time samples by inverse fast Fourier transform (IFFT).

Fig. 1 illustrates the IFFT of a group of N complex coefficients $A_1.e^{j\varphi 1}$ to $A_N.e^{j\varphi N}$. Each coefficient $A_i.e^{j\varphi i}$, where i is included between 1 and N, is associated with a respective frequency or tone f_i. The transform of a coefficient $A_i.e^{j\varphi i}$ is a sequence of digital samples in the time field, forming a section of a sinusoidal carrier of frequency f_i, of amplitude A_i, and of phase φ_i. A first curve shows a sinusoid section of amplitude A_1, of period $1/f_1$ and of phase φ_1, obtained by IFFT of a coefficient $A_1.e^{j\varphi 1}$ associated with a frequency f_1. A second and a third curves show sections of sinusoids obtained by IFFT of coefficients $A_2.e^{j\varphi 2}$ and $A_N.e^{j\varphi N}$, respectively associated with frequencies f_2 and f_N.

An IFFT of the group of coefficients $A_i.e^{j\varphi i}$ is formed by the sum of the sections of sinusoidal carriers obtained by IFFT of each of coefficients $A_i.e^{j\varphi i}$ for i included between 1 and N, this sum being called a "symbol". The IFFT of N coefficients provides a symbol D_t formed of a succession of N complex digital samples S_1 to S_N. It should be noted that the shape of the symbol D_t shown is not realistic, but aims at simplifying the understanding of the present description.

The time samples obtained by IFFT are converted into analog to be transmitted, for example, by a telephone line. On the receive side, the analog signal of the line is converted into digital, and the resulting samples are converted into complex frequency coefficients by fast Fourier transform (FFT).

To suppress a number of problems due to interference between symbols appearing upon transmission of the symbols, a "cyclic prefix" (or guard interval) is interposed before each symbol. The cyclic prefix is the reproduction at the beginning of a symbol of the last samples of this symbol.

Fig. 2 shows a conventional circuit 10 of introduction of a cyclic prefix of τ samples. The complex coefficients $A_i.e^{j\varphi i}$ for $i \in [1, N]$ are provided to an IFFT circuit 12. IFFT circuit 12 generates from the group of complex coefficients a symbol D_t comprised of N time samples S_1 to S_N. Symbol D_t is provided to a memory of FIFO type 14 and to a first input of a multiplexer 16. The output of memory 14 is connected to a second input of multiplexer 16.

At a time t_1, IFFT circuit 12 provides a first sample S_1 of symbol D_t, and memory 14 is controlled in the write mode to store this sample and the following. Multiplexer 16 is switched to select the output of memory 14, which provides a sample of a preceding symbol. This configuration of circuit 10 remains unchanged until a time $t_{N-\tau}$.

At time $t_{N-\tau}$, memory 14 has ended providing the samples of the preceding symbol and it contains the samples of the current symbol D_t, to the last sample preceding the cyclic prefix. IFFT circuit 12 starts providing the prefix samples, which samples, designated as S_I to S_N, continue being stored in memory 14. Meanwhile, multiplexer 16 is switched so that it transmits these prefix samples S_I to S_N. This configuration of circuit 10 remains unchanged until a time t_N.

At time t_{N+1}, IFFT circuit 12 is stopped, memory 14 contains the entire current symbol D_t and the prefix has just been transmitted. Multiplexer 16 is switched again to transmit the samples S_1 to S_N provided by memory 14, that is, symbol D_t.

At a time $t_{N+\tau+1}$, IFFT circuit 12 is reactivated and it starts providing the samples of the next sample. Time $t_{N+\tau+1}$ corresponds for the next symbol to previously-described time t_1.

This configuration of circuit 10 remains unchanged until a time $2t_N$ when symbol D_t will have been transmitted after its cyclic prefix.

Time $2t_{N+1}$ corresponds for the next symbol to previously-described time $t_{N-\tau}$.

A major disadvantage of circuit 10 is that the introduction of the cyclic prefix results in a delay t_N (of N samples) in the transmission of symbol D_t. In some applications, such as telephone communications or other real time communications, the introduction of such a delay is not acceptable.

Besides, in prior art circuit 10, since the number N of samples may be high, memory 14 may have a large size.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a cyclic prefix generation circuit that introduces a particularly low transmission delay.

Another object of the present invention is to provide such a circuit that uses a memory of reduced size.

To achieve these objects, the present invention provides a circuit for generating a cyclic prefix of a symbol comprised of a sequence of time samples, said prefix being the reproduction of the last samples of the symbol at the beginning of the symbol, the symbol being obtained by inverse Fourier transform of complex coefficients corresponding to respective frequencies, including means for shifting the phase of each complex coefficient by a value proportional to its frequency, a memory for storing the samples of the beginning of the symbol, and means for copying at the end of the symbol the stored samples.

According to an embodiment of the present invention, the means for shifting the phase of the complex coefficients include a multiplier connected to multiply each complex

coefficient by a complex value having a unity norm and a phase proportional to the frequency associated with each coefficient.

According to an embodiment of the present invention, the memory is of FIFO type.

According to an embodiment of the present invention, the means for copying the stored samples include a multiplexer, a first input and a second input of which are respectively connected to the input and to the output of the memory.

The present invention further aims at a method for generating a cyclic prefix of a time symbol, said prefix being the reproduction of the last samples of the symbol at the beginning of the symbol, the symbol being obtained by inverse Fourier transform of complex coefficients corresponding to respective frequencies, that includes the steps of shifting the phase of each complex coefficient by a value proportional to the frequency with which it is associated, storing the samples of the beginning of the symbol, and copying the stored samples at the end of the symbol.

The foregoing objects, features and advantages of the present invention will be discussed in detail in the following non-limiting description of specific embodiments in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1, previously described, illustrates an IFFT of a group of complex coefficients;

Fig. 2, previously described, illustrates the generation of a cyclic prefix by means of a circuit according to prior art;

Fig. 3 illustrates an IFFT of a group of complex coefficients according to the present invention; and

Fig. 4 illustrates an embodiment of a cyclic prefix generation circuit according to the present invention.

DETAILED DESCRIPTION

The present invention provides circularly shifting the samples of a symbol to which a cyclic prefix is desired to be added, this so that the last samples forming the symbol before shifting are at the beginning of the symbol after shifting, and thus directly form the prefix. By transmitting the symbol thus shifted, the prefix is first transmitted, followed by a portion of the symbol which only needs be completed by the prefix to restore the symbol. Thus, a delay equal to the prefix only is introduced in the transmission and it is sufficient to only store the prefix to be able to retransmit it to complete the symbol.

The circular shifting of the symbol must correspond to a same circular shifting of all the sinusoids that form the symbol. For this purpose, each complex frequency coefficient is multiplied by a complex factor causing a time shift, corresponding to the desired circular shift.

Fig. 3 is intended for illustrating this procedure in further detail. It illustrates the IFFT of a group of N complex coefficients $A_1.e^{j\varphi 1}$ to $A_N.e^{j\varphi N}$ multiplied according to the present invention by respective shifting coefficients $e^{jK_1\tau}$ to $e^{jK_N\tau}$. Multiplying a coefficient $A_i.e^{j\varphi i}$ by a complex coefficient $e^{j\Delta\varphi}$ amounts to modifying the phase φ_i by a value $\Delta\varphi$. Phase shift $\Delta\varphi$ causes a circular shifting of the corresponding sinusoid section by a value $\Delta\varphi/2\pi f_i$, where f_i is the frequency of the sinusoid section. This shift is not constant, but is a function of frequency f_i.

According to the present invention, the N complex coefficients $A_1.e^{j\varphi 1}$ to $A_N.e^{j\varphi N}$ are phase-shifted so that the corresponding sinusoid sections are all circularly shifted by a same value, or by the same number τ of samples. For this purpose, each coefficient $A_i.e^{j\varphi i}$ is multiplied by a coefficient $e^{jK_i\tau}$, where K_i is $2\pi f_i$. Thus, symbol D_t' formed of the sum of the sinusoid sections corresponding to coefficients $A_i.e^{j\varphi i}.e^{jK_i\tau}$, where i varies from 1 to N, corresponds to the preceding symbol D_t having undergone a circular shifting by τ samples.

Coefficients $e^{jK_i\tau}$ are predetermined, and they can for example be stored in a ROM.

Fig. 4 shows an embodiment of a circuit 20 for generating a cyclic prefix according to the present invention. This circuit is similar to that of Fig. 2, and same references designate same elements. According to the present invention, complex coefficients $A_i.e^{j\varphi i}$ for $i\in[1, N]$ are provided to IFFT circuit 12 via a complex multiplier 22, a second input of which correspondingly receives the above-mentioned N coefficients $e^{jK_i\tau}$.

As seen in relation with Fig. 3, symbol D_t' provided by the IFFT circuit of Fig. 4 corresponds to symbol D_t of Fig. 2 having undergone a circular shifting by τ samples. Thus, samples S_1' to S_J' of the first τ times of symbol D_t' are samples S_I to S_N of the last τ times of symbol D_t. Samples S_1' to S_J' of symbol D_t' form the cyclic prefix of symbol D_t, and the following samples of symbol D_t' form the T-τ first samples of symbol D_t. To complete symbol D_t, it is enough to copy samples S_1' to S_J' after symbol D_t'. To achieve this, samples S_1' to S_J' will have been stored in memory 24, which memory must only store τ samples instead of N-τ.

At a time t_1, IFFT circuit 12 provides the first sample S_1' of symbol D_t', and memory 24 is controlled in the write mode to store the samples generated by the IFFT circuit. Multiplexer 16 is switched to select the output of IFFT circuit 12. This configuration of circuit 10 remains unchanged until a time t_τ; it enables storing samples S_1' to S_J' in memory 24 and providing at the output of multiplexer 16 the cyclic prefix, formed by samples S_1' to S_J'.

At time $t_{\tau+1}$, memory 24, which has just stored samples S_1' to S_J', is deactivated. The position of multiplexer 16 is not modified, and this configuration of circuit 10 is maintained until a time t_N. Multiplexer 16 provides in this interval samples S_{J+1}' to S_N' of symbol D_t', which correspond to previously described samples S_1 to S_I.

At time t_{N+1}, IFFT circuit 12 is stopped, memory 24 is controlled in the read mode to provide the first sample S_1' that it contains, and multiplexer 16 is switched to select the output of memory 24. This configuration of circuit 10 remains unchanged until a time $t_{N+\tau}$. In this interval, multiplexer 16 successively provides samples S_1' to S_J' read from memory 24, which correspond to above mentioned samples S_{I+1} to S_N.

At time $t_{N+\tau+1}$, IFFT circuit 12 is reactivated to provide the samples of the next symbol and the cycle just described is resumed as at time t_1.

The present invention enables generating the cyclic prefix of a symbol by only delaying the symbol by duration τ of the prefix. This is a time gain of $t_{N-\tau}$ with respect to prior art, which is particularly valuable in the case of real time transmissions.

Further, memory 24 used according to the present invention is of reduced size, since it is used to only store the samples forming the prefix.

Of course, the present invention is likely to have various alterations, modifications, and improvements which will readily occur to those skilled in the art. Such alterations, modifications, and improvements are intended to be part of this disclosure, and are intended to be within the spirit and the scope of the present invention. Accordingly, the foregoing description is by way of example only and is not intended to be limiting. The present invention is limited only as defined in the following claims and the equivalents thereto.